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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/537,274	03/29/2000	Larry Eugene Mosley	884.240US1	7167

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EXAMINER

THOMAS, ERIC W

ART UNIT PAPER NUMBER

2831

DATE MAILED: 10/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/537,274

Applicant(s)

MOSLEY, LARRY EUGENE

Examiner

Eric W Thomas

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 July 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 9, 10 and 14-18 is/are allowed.
- 6) ☒ Claim(s) 1-5, 8, 11, 13, 19 and 21 is/are rejected.
- 7) ☒ Claim(s) 6, 7, 12 and 20 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

DETAILED ACTION**Introduction:**

The examiner acknowledges, as recommended in the M.P.E.P., the applicant's submission of the amendment dated 7/15/02. At this point claim 1 has been amended. Claims 1-21 are pending in the instant application.

Claim Rejections - 35 USC § 102

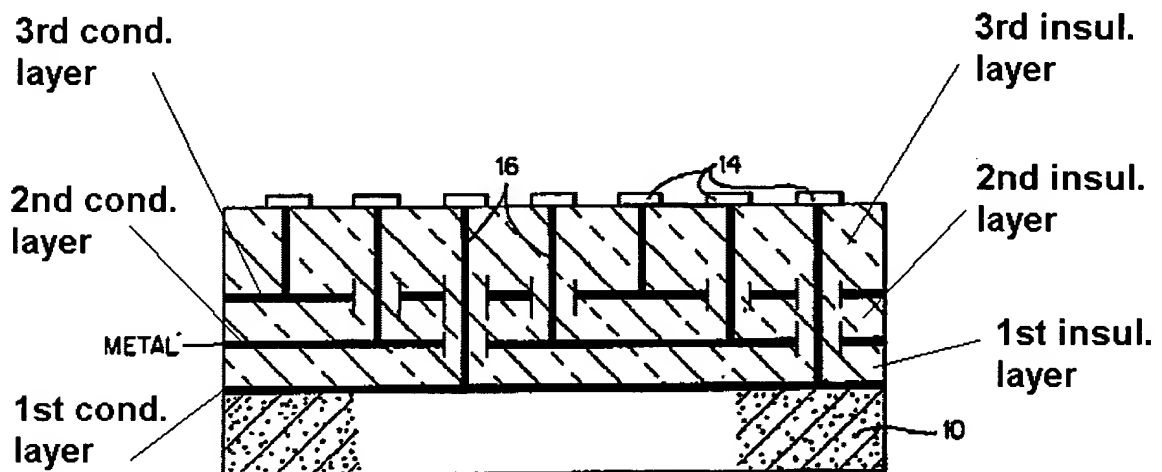
1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 8, 11 are rejected under 35 U.S.C. 102(b) as being anticipated by IBM

Technical disclosure bulletin (Cross-reference 0018-8689-20-8-3117 – Referred as '3117).

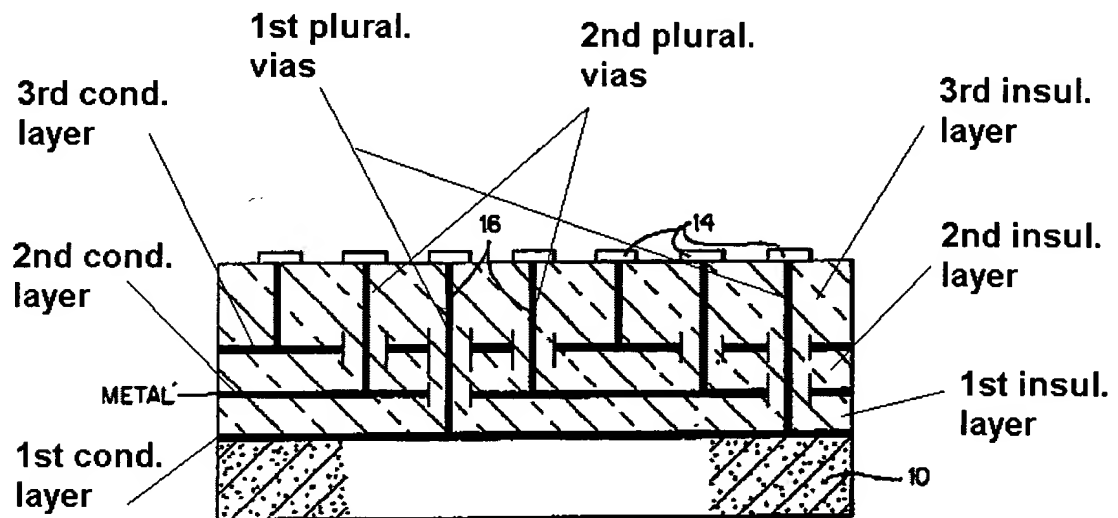


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'3117 discloses a multi layer integrated circuit capacitor comprising: a substrate (10); a first conductive layer located over and contacting the substrate (see above);

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate; a second conductive layer located over the first insulator layer; a second insulator layer located over the second conductive layer; a third conductive layer located over the second insulator layer; a third insulator layer located over the third conductor layer; and a plurality of conductive vias (16) downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductive layers.

Regarding claim 8, '3117 discloses some of the plurality of conductive vias pass through the second conductive layer without forming an electrical connection with the second conductive layer (see above fig).



Regarding claim 11, '3117 disclose a multi layer integrated circuit capacitor comprising: a substrate (10); a first conductive layer located over and contacting the

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substrate; a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate; a second conductive layer located over the first insulator layer, the second conductive layer being fabricated as a plurality of laterally spaced strips such that a surface area of the second conductive layer is less than a surface area of the first conductive layer; a second insulator layer located over the second conductive layer; a third conductive layer located over the second insulator layer, the third conductive layer being fabricated as a plurality of laterally spaced strips such that a surface area of the third conductive layer is less than the surface area of the second conductive layer; a third insulator layer located over the third conductive layer; a first plurality of conductive vias (16) downwardly extending through the third insulator layer to provide electrical interconnection to the third conductive layer; a second plurality of conductive vias (16) downwardly extending through the third insulator layer to provide electrical interconnection to the second conductive layer; and a third plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first conductive layer (SEE ABOVE).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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4. Claims 4-5, 13, 19, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over IBM Technical disclosure bulletin (Cross-reference 0018-8689-20-8-3117 – Referred as '3117).

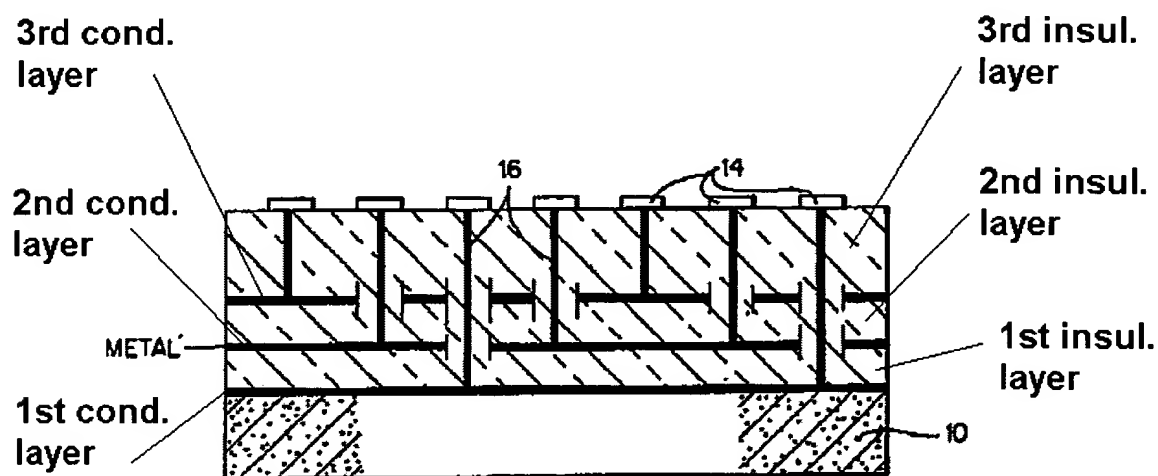
Regarding claim 4, '3117 discloses the claimed invention except for the insulator layers are formed from a BaSrTiO₃ material. It is well known in the capacitor art to form insulating layers from a BaSrTiO₃ material (excellent dielectric properties). It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the dielectric from a BaSrTiO₃, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding claim 5, '3117 discloses the claimed invention for the conductive layers are formed from copper. It is well know in the capacitor art to form conductive layers (electrodes) from a copper material (excellent conductive properties). It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the conductive layers from a copper material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding claim 13, '3117 discloses the claimed invention except for the insulator layers are formed from a BaSrTiO₃ material. It is well known in the capacitor art to form insulating layers from a BaSrTiO₃ material (excellent dielectric properties). It would have been obvious to one having ordinary skill in the art at the time the invention

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was made to form the dielectric from a BaSrTiO₃, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.



Regarding claim 19, '3117 discloses a multi layer integrated circuit capacitor comprising: a substrate (10); a first conductive layer located over and contacting the substrate (see above); a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate; a second conductive layer located over the first insulator layer; a second insulator layer located over the second conductive layer; a third conductive layer located over the second insulator layer; a third insulator layer located over the third conductor layer; and a plurality of conductive vias (16) downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductive layers.

'3117 discloses the claimed invention except for the plurality of vias extending through the substrate to provide electrical interconnection to both a top surface and a bottom surface of the integrated circuit capacitor. It is well known in the capacitor art to extend vias through a substrate to provide electrical interconnections to both sides of the capacitive element. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to extend the vias of '3117 through the substrate to provide electrical interconnections to both sides of the capacitor, since such a modification would decrease the space needed in the electrical system.

Regarding claim 21, '3117 discloses the claimed invention for the conductive layers are formed from copper. It is well known in the capacitor art to form conductive layers (electrodes) from a copper material (excellent conductive properties). It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the conductive layers from a copper material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

5. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over IBM Technical disclosure bulletin (Cross-reference

6. 0018-8689-20-8-3117 – Referred as '3117) in view of Herrell (US 6,191,479).

'3117 disclose the claimed invention (as seen in claim 1) except for a plurality of controlled collapse chip connection (C4) lands fabricated on and contacting the third insulator layer and in electrical contact with the plurality of conductive vias. '3117

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illustrates voltage supply pads formed on and contacting the third insulator layer and in electrical contact with the plurality of conductive vias. The capacitor is connected to a chip by short metal lines (see fig. 2).

Herrell teaches the use of C4 lands that electrically contacts vias in the capacitor art. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the capacitor of '3117 using the C4 lands as taught by Herrell, since such a modification would decrease the space used in the electrical system by placing the capacitor directly onto the chip.

Regarding claim 3, '3117 disclose the claimed invention except for C4 lands fabricated in staggered columns in a plan view. '3117 illustrates a column of voltage supply pads arranged on a capacitor. Herrell illustrates multiple C4 lands fabricated in staggered columns in a plan view. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form multiple C4 lands which is fabricated in staggered columns in a plan view, since such a modification would allow additional connections to the capacitor of '3117.

Response to Arguments

7. Applicant's arguments with respect to claims 1-5, 11, 13, 19, 21, have been considered but are moot in view of the new ground(s) of rejection.

8. Claims 9-10, 14-18 are allowed.

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9. Claims 6-7, 12, 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric W Thomas whose telephone number is (703) 305-0878. The examiner can normally be reached on Mon & Sat 9:00AM - 9:30PM; Tues-Fri 5:30PM-10:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 703-308-3682. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

ewt
October 17, 2002

ANTHONY DINKINS
PRIMARY EXAMINER

A handwritten signature in cursive script that reads "Anthony Dinkins". The signature is written in black ink and is positioned below the printed name and title.